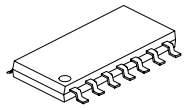
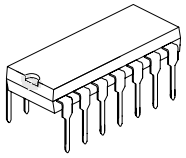
U74HC14

CMOS IC

HIGH-SPEED CMOS LOGIC HEX INVERTING SCHMITT TRIGGER



SOP-14



DIP-14

*Pb-free plating product number: U74HC14L

■ DESCRIPTION

The UTC **U74HC14** each contain six inverting Schmitt triggers in one package. Each of them perform the Boolean function $Y=\overline{A}$.

■ FEATURES

* Widely range of input rise and fall time
* high noise immunity
* Fan-out parameters(over temperature range) up to 10 LSTTL Loads
* Low power consumption
* Wide range operation 2V ~ 6V

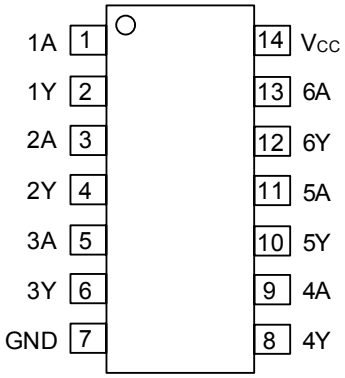
■ ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead Free Plating		
U74HC14-D14-T	U74HC14L-D14-T	DIP-14	Tube
U74HC14-S14-R	U74HC14L-S14-R	SOP-14	Tape Reel
U74HC14-S14-T	U74HC14L-S14-T	SOP-14	Tube

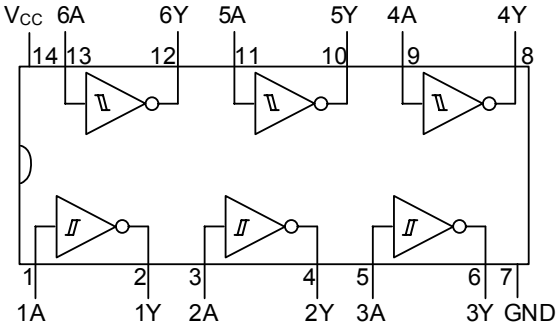
U74HC14L-D14-T
(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) R: Tape Reel, T: Tube
(2) D14: DIP-14, S14: SOP-14
(3) L: Lead Free Plating, Blank: Pb/Sn

■ PIN CONFIGURATION



■ FUNCTIONAL DIAGRAM

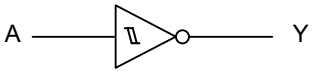


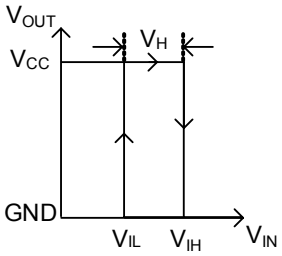
■ TRUTH TABLE

INPUT(A)	OUTPUT(Y)
L	H
H	L

H=High level
L=Low Level

■ LOGIC DIAGRAM





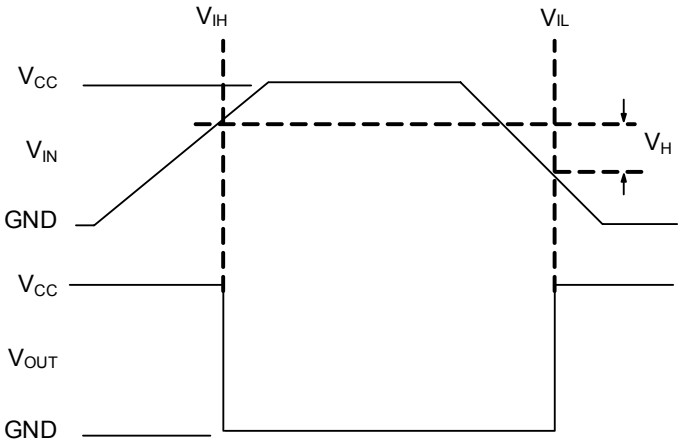


Figure 1. Hysteresis Definition, Characteristic, And Test Setup

■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
DC Supply Voltage		V_{CC}	-0.5V~9V	V
DC Input Clamp Current	For V_{IN} < -0.5V or V_{IN} > V_{CC} + 0.5V	I_{IK}	±20mA	mA
DC Output Clamp Current	For V_{OUT} < -0.5V or V_{OUT} > V_{CC} + 0.5V	I_{OK}	±20mA	mA
DC Drain Current, per Output	For -0.5V < V_{OUT} < V_{CC} +0.5V	I_{OUT}	±25mA	mA
DC Output Source or Sink Current Per Output Pin	For V_{OUT}> -0.5V or V_{OUT} < V_{CC} + 0.5V	I_{OUT}	±25mA	mA
DC V_{CC} or Ground Current		I_{CC}	±50mA	mA
Operating Conditions				
Supply Voltage Range HC Types		V_{CC}	0V~V_{CC}	V
DC Input or Output Voltage		V_{IN}, V_{OUT}	0V~V_{CC}	V
Operating Temperature		T_A	-40~ +85℃	V
Storage Temperature		T_{STG}	-65 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction Ambient	θ_{JA}	86	℃/W

■ ELECTRICAL CHARACTERISTICS (T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Switch Points	V_{IH}	V_{CC}=2V	0.7	1.2	1.5	V
		V_{CC}=4.5V	1.55	2.5	3.15	V
		V_{CC}=6V	2.1	3.3	4.2	V
	V_{IL}	V_{CC}=2V	0.3	0.6	1	V
		V_{CC}=4.5V	0.9	1.6	2.45	V
		V_{CC}=6V	1.2	2	3.2	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IN}=V_{IH} or V_{IL}, V_{CC}=2V, I_{OUT}=-0.02mA	1.9			V
		V_{IN}=V_{IH} or V_{IL}, V_{CC}=4.5V, I_{OUT}=-0.02mA	4.4			V
		V_{IN}=V_{IH} or V_{IL}, V_{CC}=6V, I_{OUT}=-0.02mA	5.9			V
High Level Output Voltage TTL Loads		V_{IN}=V_{IH} or V_{IL}, V_{CC}=4.5V, I_{OUT}=-4 mA	3.98			V
		V_{IN}=V_{IH} or V_{IL}, V_{CC}=6V, I_{OUT}=-5.2 mA	5.48			V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IN}=V_{IH} or V_{IL}, V_{CC}=2V, I_{OUT}=0.02 mA			0.1	V
		V_{IN}=V_{IH} or V_{IL}, V_{CC}=4.5V, I_{OUT}=0.02 mA			0.1	V
		V_{IN}=V_{IH} or V_{IL}, V_{CC}=6V, I_{OUT}=0.02 mA			0.1	V
Low Level Output Voltage TTL Loads		V_{IN}=V_{IH} or V_{IL}, V_{CC}=4.5V, I_{OUT}=4 mA			0.26	V
		V_{IN}=V_{IH} or V_{IL}, V_{CC}=6V, I_{OUT}=5.2 mA			0.26	V
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} and GND, V_{CC}=6V			±0.1	μA
Quiescent Device Current	I_{CC}	V_{IN}=V_{CC} or GND, V_{CC}=6V, I_{OUT}=0			2	μA

Note 1. For dual-supply systems theoretical worst case (V_{IN} = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

■ SWITCHING SPECIFICATIONS (T_A = 25°C, Input t_R, t_F = 6ns)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Propagation Delay, A to Y	t_{PLH}, t_{PHL}	V_{CC}=2V, C_L=50pF	2			40	ns
		V_{CC}=4.5V, C_L=50pF	4.5			24	ns
		V_{CC}=6V, C_L=50pF	6			22	ns
Output Transition Times	t_{TLH}, t_{THL}	V_{CC}=2V, C_L=50pF	2			19	ns
		V_{CC}=4.5V, C_L=50pF	4.5			16	ns
		V_{CC}=6V, C_L=50pF	6			15	ns
Input Capacitance	C_{IN}					10	pF
Power Dissipation Capacitance (Notes 2, 3)	C_{PD}	V_{CC}=5V,	5		20		pF

Note 2. C_{PD} is used to determine the dynamic power consumption, per inverter.

3. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

■ TEST CIRCUITS AND WAVEFORMS

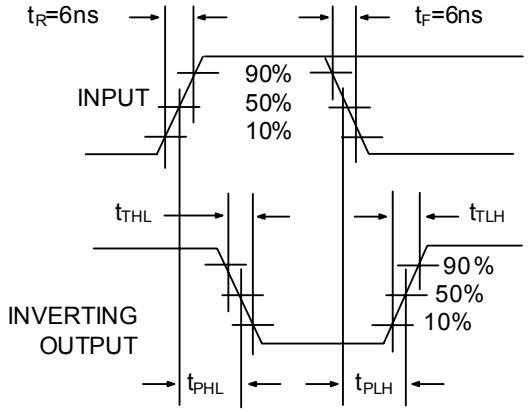


Figure 2. U74HC14 Transition Times And Propagation Delay Times, Combination Logic